Status of Claims

Claims 1 and 3-9 are pending.

Claims 1 and 3-9 stand rejected.

Claims 1, 4 and 5 have been amended.

Claim 3 has been canceled and its subject matter incorporated into claims 1 and 5.

No new matter has been introduced into the Application by these amendments.

Remarks/Arguments

The Examiner is thanked for the June 27, 2011 telephone interview, and for the proposed amendments made therein for moving the case into a condition for allowance. By way of this response, the amendments proposed by the Examiner relating to the outstanding art rejections have been incorporated into the independent claims.

Claim Rejections – 35 U.S.C. § 101

Claims 1, 3 and 4 stand rejected under 35 U.S.C. § 101 as allegedly directed to non-statutory subject matter. This rejection is respectfully traversed. As amended herein, method claim 1 recites:

> A method for accelerating *a pseudo-random input bit flow having a length of* 2^{n-1} *bits, generated from a polynomial of an irreducible degree n* at a *first clock frequency*, into an *identical output bit flow* at a *second clock frequency, greater than the first clock frequency*, the method comprising:
>
> *collecting* the *output bit flow*;
>
> *delaying* the *collected* flow by a predetermined value (τ) respecting the following relation:

> $\tau = ((2^{\ell})*T_1)-T_0$,
>
> wherein T_1 *represents the clock period of the input bit flow*, T_0 *represents the clock period of the output bit flow*, and ℓ is a non-zero integer setting a decimation parameter,
>
> wherein delay τ is also selected to respect the following relation:
>
> $\tau = (2k+1)*(2^n-1)*T_0$,
>
> where k represents any non-zero integer, and where n represents the degree of the irreducible polynomial of the random sequence, and
>
> *combining via a recirculation loop*, the *delayed flow with* the *input bit flow* to generate the *output bit flow at* the *second clock frequency*. (*emphasis added*)

In the first instance, it is respectfully submitted that no rational basis exists for rejection of present claim 1 under 35 U.S.C. § 101 as directed to non-statutory subject matter. Method claim 1 does not describe an abstract idea, a natural phenomenon, a law of nature, nor does it fail to recite a practical application of such judicial exceptions. More particularly, present claim 1 *does not* merely recite a general disembodied concept of delaying an input and combining the delayed input to generate an output, as suggested by the Examiner on page 2 of the Final Office Action. In contradistinction, claim 1 recites a method that transforms *a pseudo-random input bit flow having a length of* 2^{n-1} *bits, generated from a polynomial of an irreducible degree n* at a first *clock* frequency, into an *identical output bit flow* but whose frequency is at a second *clock* frequency greater than the *clock* frequency of the input bit flow. This is accomplished, inter alia, by *collecting* the output bit flow and then *delaying* the *collected* output bit flow by a particular delay as given by $\tau = ((2^{\ell})*T_1)-T_0$, wherein T1 *represents the clock period of the input bit flow*, T0 *represents the clock period of the output bit flow*, and ℓ is a non-zero integer setting a decimation parameter. The delay τ is further embodied to respect the following

relation: $\tau = (2k+1)*(2n-1)*T0$, where k represents any *non-zero* integer, and where n represents the degree of the irreducible polynomial of the *random sequence clock period*. Still further, the claimed method requires the *combining via a recirculation loop*, the *delayed flow* from the *collected* output *with* the *input bit flow* to generate the *output bit flow at* the *second clock frequency*. As discussed in paragraph [0048] of the published application, "*the present invention forms a recirculation loop in which the delay is applied to a signal collected at the output*".

Accordingly, the invention as claimed in present claim 1 is more than a general disembodied concept in which the mechanisms by which the steps are implemented are subjective. Rather, the claimed method represents a practical application for generating random bit trains which enables achieving high bit rates (see paragraph [0012]) according to the output collecting, delaying, and combining steps. Furthermore, the combining step is implemented via a recirculation loop that additionally ties the method steps to a tangible article. In view of the foregoing, present claim 1 fully meets the requirements of 35 USC 101. Reconsideration and withdrawal of this 35 U.S.C. § 101 rejection is respectfully requested.

Claim Rejections – 35 U.S.C. § 102

Claims 1 and 5-9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ailett et al. (U.S. Patent No. 3,881,099, hereinafter Ailett). Applicant respectfully traverses this rejection for at least the reasons set forth below.

As indicated above, in order to expedite allowance of the present application, independent claims 1 and 5 have been amended in accordance with the Examiner's proposed amendment of June 27, 2011. Specifically, claims 1 and 5 have been amended to:

1.) specify that ℓ is a non-zero integer;

2.) incorporate the subject matter of claim 3 into claim 1; and

3.) specify that k is a non-zero integer.

Accordingly, Applicant respectfully submits claims 1 and 5 should be allowable over the cited prior art. Claims 6-9 should be allowable at least by virtue of their ultimate dependence from claim 5.

These amendments have been made without prejudice or disclaimer, and, without limitation, without prejudice to the right of Applicant to introduce claims identical to or similar to original claims 1 and 5, and any of their dependent claims, in one or more continuation or continuation-in-part applications claiming benefit of the present application. Without limitation, the present amendments do not reflect agreement or admission by Applicant as to the characterization of the prior art in the Office Action.

Reconsideration and withdrawal of the 35 U.S.C. § 102 rejection of claims 1 and 5-9 is respectfully requested.

Claim Rejections – 35 U.S.C. § 103

Claims 3-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ailett. Applicant respectfully traverses this rejection and submits that these claims are patentable over the cited art of record for at least the reasons set forth below.

Claim 3 has been canceled, and its subject matter incorporated into claim 1 according to the Examiner's proposed amendment. Claim 4 has been amended to depend from claim 1, and should be allowable at least by virtue of this dependency.

In view of the foregoing, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection of claims 3 and 4.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Conclusion

Applicant believe he has addressed all outstanding grounds raised by the Examiner and respectfully submits the present case is in condition for allowance, early notification of which is earnestly solicited.

Should there be any questions or outstanding matters, the Examiner is cordially invited and requested to contact Applicant's undersigned attorney at his number listed below.

Respectfully submitted,

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